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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/973,058	10/10/2001	Toshio Sakurai	03500.015866.	5036

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FITZPATRICK CELLA HARPER & SCINTO
30 ROCKEFELLER PLAZA
NEW YORK, NY 10112

EXAMINER	
MILIA, MARK R	

ART UNIT	PAPER NUMBER
2625	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/973,058	SAKURAI, TOSHIO	
	Examiner	Art Unit	
	Mark R. Milia	2625	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 December 2008 and 11 March 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's amendments were received on 12/12/08 and 3/11/09 and have been entered and made of record. Currently, claims 1-10 are pending.

Response to Arguments

2. Applicant's arguments filed 12/12/08 and 3/11/09 have been fully considered but they are not persuasive.

Applicant asserts that Wakasugi et al. (US 5,961,616) is not seen to disclose or suggest a second circuit for determining whether information currently latched by a first circuit is the same as information latched by the first circuit a previous time, thereby determining whether or not the currently latched information matches a predetermined protocol, wherein in the second circuit, if it is determined that the information currently latched by the first circuit is the same as the information latched by the first circuit the previous time, the second circuit determines that the information currently latched by the first circuit does not match the predetermined protocol and therefore skips processing of the currently latched information, and wherein in the second circuit, if it is determined that the information currently latched by the first circuit is not the same as the information latched by the first circuit the previous time, the second circuit determines

that the information currently latched by the first circuit matches the predetermined protocol and therefore outputs the currently latched information to be processed. The examiner respectfully disagrees as Wakasugi does disclose such features. Particularly, Wakasugi states, in reference to Fig. 10, in order to produce a state resumption signal, there are provided an 8-bit data buffer 40 serving as a third data buffer which stores a previous transferred data D0 to D7, a 1-bit data buffer 41 serving as a third strobe signal buffer, which stores the status of a previous strobe signal, an 8-bit comparator 42 which receives the contents of the current transferred data D0 to D7 and the contents of the previous transferred data D0 to D7, delivering a "1" upon coincidence therebetween, a 1-bit comparator 43 receiving the status of the current strobe signal and the status of the previous strobe signal, and delivering a "1" upon coincidence therebetween, an AND gate 44 for receiving outputs from the 8-bit comparator 42 and the 1-bit comparator 43 to form a logical product thereof and delivering it to the sequence circuit 25 as a state resumption signal. The contents of the 8-bit data buffer 40 and the 1-bit data buffer 41 are updated in synchronism with the rising edge of the internal strobe signal which is output from the sequence circuit 25. The state resumption signal assumes a "1" upon coincidence between the contents of the previous and the current transferred data D0 to D7, and upon coincidence between the status of the previous and the current strobe signals which is indicative of a **spike noise condition** (column 11 lines 32-55). Thus, as long as the data changes in association with a predetermined protocol, the data will be output appropriately, but if a “spike noise” is detected based on

the current and previous transferred data and the previous and current strobe signal, then the "spike noise" is invalidated and not output.

Claim Rejections - 35 USC § 102

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims 1, 2, 4, 6, and 7 are rejected under 35 U.S.C. 102(b) as being anticipated by Wakasugi (US 5,961,616).

Regarding claims 1 and 6, Wakasugi discloses an interface apparatus and information processing method to which information is input from an external apparatus according to a predetermined protocol which does not continuously transmit the same information comprising: a first circuit for waiting until a predetermined time has elapsed from a time when the information input from the external apparatus has changed, and latching the information input from the external apparatus in response to the elapse of the predetermined time (see Figs. 10-12 and column 9 lines 41-43, column 10 lines 42-46, column 11 lines 32-55, and column 12 lines 60-63, transferred data is latched after waiting for the termination of a transition state) and a second circuit for determining whether the information currently latched by the first circuit is the same as information latched by the first circuit a previous time, thereby determining whether or not the currently latched information matches the predetermined protocol, wherein in the second circuit if it is determined that the information currently latched by the first circuit

is the same as the information latched by the first circuit the previous time, the second circuit determines that the information currently latched by the first circuit does not match the predetermined protocol and therefore skips processing of the currently latched information, and wherein in the second circuit if it is determined that the information currently latched by the first circuit is not the same as the information latched by the first circuit the previous time, the second circuit determines that the information currently latched by the first circuit matches the predetermined protocol and therefore outputs the currently latched information to be processed (see Figs. 10-12 and column 11 line 28-column 13 line 4, the contents of the 8-bit data buffer 40 and the 1-bit data buffer 41 are updated in synchronism with the rising edge of the internal strobe signal which is output from the sequence circuit 25. The state resumption signal assumes a "1" upon coincidence between the contents of the previous and the current transferred data D0 to D7, and upon coincidence between the status of the previous and the current strobe signals which is indicative of a **spike noise condition**).

Regarding claims 2 and 7, Wakasugi further discloses a data change detector for outputting a reset in the case where there is a change in the information input from the external apparatus (see Fig. 10 (10) and column 3 line 65-column 4 line 10), a timer for inputting the reset output by the change detector and outputting a trigger after the elapse of a predetermined time from the input of the reset (see Fig. 12 and column 12 lines 14-65), a data latch for inputting the trigger output by said timer and fetching the information input from the external apparatus in accordance with the input of the trigger (see Fig. 10, column 9 lines 40-63, and column 10 line 61-column 11 line 16).

Regarding claim 4, Wakasugi further discloses wherein the information which is inputted from the external apparatus is inputted to the first circuit and the information fetched by said first circuit is input to the second circuit (see Fig. 10 and column 11 line 17-column 12 line 65).

Claim Rejections - 35 USC § 103

5. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

6. Claims 5 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wakasugi in view of Motoyama (US 5,818,603).

Wakasugi discloses a first circuit for waiting until a predetermined time has elapsed from a time when the information input from the external apparatus has changed, and latching the information input from the external apparatus in response to the elapse of the predetermined time (see Figs. 10-12 and column 9 lines 41-43, column 10 lines 42-46, column 11 lines 32-55, and column 12 lines 60-63, transferred data is latched after waiting for the termination of a transition state) and a second circuit for determining whether the information currently latched by the first circuit is the same as information latched by the first circuit a previous time, thereby determining whether or not the currently latched information matches the predetermined protocol, wherein in the second circuit if it is determined that the information currently latched by the first circuit is the same as the information latched by the first circuit the previous time, the

second circuit determines that the information currently latched by the first circuit does not match the predetermined protocol and therefore skips processing of the currently latched information, and wherein in the second circuit if it is determined that the information currently latched by the first circuit is not the same as the information latched by the first circuit the previous time, the second circuit determines that the information currently latched by the first circuit matches the predetermined protocol and therefore outputs the currently latched information to be processed (see Figs. 10-12 and column 11 line 28-column 13 line 4, the contents of the 8-bit data buffer 40 and the 1-bit data buffer 41 are updated in synchronism with the rising edge of the internal strobe signal which is output from the sequence circuit 25. The state resumption signal assumes a "1" upon coincidence between the contents of the previous and the current transferred data D0 to D7, and upon coincidence between the status of the previous and the current strobe signals which is indicative of a **spike noise condition**).

Wakasugi does not disclose expressly a printer engine for printing the information output by the second circuit.

Motoyama discloses a printer engine for printing the information output by the second circuit (see Fig. 1, column 3 lines 56-57, column 7 lines 33-49, and column 8 lines 36-44).

Wakasugi & Motoyama are combinable because they are from the same field of endeavor, data monitoring and transmission.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine a printer engine for printing, as described by Motoyama, with the system of Wakasugi.

The suggestion/motivation for doing so would have been to ensure the ability to properly communicate data between a host apparatus and an output device (i.e. printer) by eliminating noise from the transferred data.

Therefore, it would have been obvious to combine Motoyama with Wakasugi to obtain the invention as specified in claims 5 and 10.

7. Claims 3 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wakasugi as applied to claims 1 and 6 above, and further in view of Motoyama.

Wakasugi does not disclose expressly wherein the external apparatus forms information such that information is non-continuous information.

Motoyama discloses wherein the external apparatus forms information such that information is non-continuous information (see column 4 lines 15-19, column 6 line 63-column 7 line 3, column 7 line 24-column 8 line 44, and column 11 lines 6-49).

Wakasugi & Motoyama are combinable because they are from the same field of endeavor, data monitoring and transmission.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine non-continuous transfer of information, as described by Motoyama, and which is well known in the art of printing, with the system of Wakasugi.

The suggestion/motivation for doing so would have been to ensure the ability to properly communicate data between a host apparatus and an output device (i.e. printer) by eliminating noise from the transferred data.

Therefore, it would have been obvious to combine Motoyama with Wakasugi to obtain the invention as specified in claims 3 and 8.

8. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wakasugi as applied to claim 6 above, and further in view of Chapman (US 6,175,603).

Wakasugi discloses the use of logic and logic filters in the execution of the invention (see column 11 line 17-column 12 line 65).

Wakasugi does not disclose expressly wherein the first step is executed by a glitch noise filter.

Chapman discloses the use of glitch noise filters to filter data information (see column 1 lines 36-59 and column 7 lines 44-53).

Wakasugi & Chapman are combinable because they are from the same field of endeavor, detection and processing of changes in transmitted information.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the use of a glitch noise filter as described by Chapman with the system of Wakasugi.

The suggestion/motivation for doing so would have been to accurately filter noise signals from incoming information.

Therefore, it would have been obvious to combine Chapman with Wakasugi to obtain the invention as specified in claim 9.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mark R. Milia whose telephone number is (571)272-7408. The examiner can normally be reached M-F 8:00am-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Moore can be reached at (571) 272-7437. The fax number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Mark R. Milia
Examiner
Art Unit 2625

/Mark R. Milia/
Examiner, Art Unit 2625

/David K Moore/
Supervisory Patent Examiner, Art Unit 2625